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06EC56

Fifth Semester B.E. Degree Examination, December 2011
Fundamental of CMOS VLSI

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain the nMOS enhancement mode transistor for different conditions of v_{ds}. **(08 Marks)**

b. Describe in detail BiCMOS fabrication in an n-well process. **(08 Marks)**

c. What are the advantages of BiCMOS process over CMOS technology? **(04 Marks)**

2 a. What is body effect? Which parameters are responsible for it? **(08 Marks)**

b. An nMOS transistor is operating in active region with following parameters V_{GS} = 3.9V, V_{th} = 1V, $\frac{W}{L}$ =100 , $\mu_n c_{ox}$ = 90 μA/r^2. Find I_D and drain to source resistance. **(05 Marks)**

c. Explain in detail regions of operation and mid-point voltage equation for CMOS inverter. **(07 Marks)**

3 a. List the λ-based design rules for CMOS. **(05 Marks)**

b. Draw the stick diagram for nMOS EX-OR gate. **(07 Marks)**

c. What is transmission gate? And design stick diagram for transmission gate. **(08 Marks)**

4 a. What is clocked CMOS gate? Where it is preferred? **(06 Marks)**

b. Two nMOS inverters are cascaded to drive capacitive load C_L = 16 C_g as shown in Fig.Q.4(b).Calculate pair delay v_{in} to v_{out} interms of τ. **(06 Marks)**

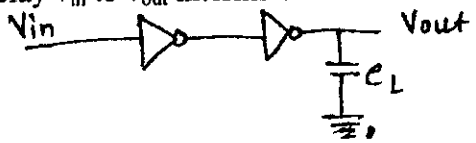

Fig.Q.4(b)

c. Find the scaling factors for MOS circuits :
i) For gate capacitance ; ii) Channel resistance (R_{on})
ii) Saturation current (Id_{ss}) ; iv) Speed power product (PT). **(08 Marks)**

PART – B

5 a. Design bus arbitration logic for n-line bus. **(10 Marks)**

b. Explain two-phase clocking generator using D flip – flops. **(10 Marks)**

6 a. Explain the design steps for 4 bit adder. **(08 Marks)**

b. Draw the basic arrangements of 4 bit serial parallel multiplier. **(08 Marks)**

c. Discuss the timing constraints for system timing considerations. **(04 Marks)**

7 a. For single phase clock define following parameters :
i) Set up time (T_s) ; ii) Hold time (T_h) ; iii) Clock to Q delay (T_q). **(03 Marks)**

b. How to read or write and hold the bit in SRAM cell? **(09 Marks)**

c. Explain the working of 1-transistor DRAM cell. Give the difference between SRAM and DRAM. **(08 Marks)**

8 a. Discuss the meaning of "REAL ESTATE" in VLSI design. **(04 Marks)**

b. What are the different types of I/O pads? **(06 Marks)**

c. List the ground rules for a system design. **(10 Marks)**

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